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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,039	03/06/2001	Pervez Hassan Sagarwala	93-C-091C1 (STMI01-00012)	7946

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	13

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/800,039	Applicant(s) SAGARWALA et al.
	Examiner Prenty	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 29, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7 and 27-39* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *1-7 and 33-39* is/are allowed.

6) ☒ Claim(s) *27-29* is/are rejected.

7) ☒ Claim(s) *30-32* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

This non-final Office Action is in response to the papers filed May 29, 2003.

The amendment filed May 29, 2003 has been entered.

Claims 27-29 are rejected under 35 U.S.C. §102(e) as being anticipated by Chen (United States Patent 5,766,991 submitted in the Information Disclosure Statement filed May 24, 2001).

With respect to independent claim 27, Chen discloses a CMOS integrated circuit structure (see the entire patent, particularly the Figs. 11-13 embodiment), comprising: an n-channel transistor including lightly doped (n^-) source and drain regions within a p-type region 10 of a substrate 14; and a p-channel transistor without lightly doped source and drain regions within an n-type region 12 of the substrate, the p-channel transistor including: a gate electrode 28 having a width less than a channel length of a channel for the p-channel transistor; and first and second sidewall spacer regions (see Fig. 12 and note column 3, lines 52-62, OR see Fig. 13's unnumbered gate sidewall oxide alone) adjacent opposing sides of the gate electrode and overlying a portion of the channel for the p-channel transistor and portions of source and drain regions 74 and 75 for the p-channel transistor.

Claim 27 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to independent claim 28, Chen discloses a CMOS integrated circuit structure (see the entire patent, particularly the Figs. 11-13 embodiment), comprising: an n-channel transistor including lightly doped (n^-) source and drain regions within a p-type region 10 of a substrate 14; and a p-channel transistor without lightly doped source and drain regions within an n-type region 12 of the substrate,

the p-channel transistor including: a gate electrode 28 having a width less than a channel length of a channel for the p-channel transistor; and first and second sidewall spacer regions (see Fig. 12 and note column 3, lines 52-62, OR see Fig. 13's unnumbered gate sidewall oxide alone) adjacent opposing sides of the gate electrode and overlying a portion of the channel for the p-channel transistor and portions of source and drain regions 74 and 75 for the p-channel transistor, wherein the width of the gate electrode 28 is less than "a minimum channel length required for the p-channel transistor" (Chen's p-channel transistor is presumed to be operative and thus its channel length between source/drain regions 74 and 75 is at least "a minimum channel length required for the p-channel transistor.")

Claim 28 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 29, Chen's first sidewall spacer regions have a width which, taken on opposing sides of the gate electrode 28 and combined with the width of the gate electrode, exceeds "the minimum channel length required for the p-channel transistor" (again, Chen's p-channel transistor is presumed to be operative and thus its channel length between source/drain regions 74 and 75 is at least "a minimum channel length required for the p-channel transistor").

Claim 29 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

Claim 30 is objected to as being dependent on a rejected base claim (i.e., claim 30 would be allowable over the prior art of record if amended to further include all the limitations of independent claim 28 and dependent claim 29).

Claim 31 is objected to as being dependent on a rejected base claim (i.e., claim

31 would be allowable over the prior art of record if amended to further include all the limitations of independent claim 28, dependent claim 29 and dependent claim 30).

Claim 32 is objected to as being dependent on a rejected base claim (i.e., claim 32 would be allowable over the prior art of record if amended to further include all the limitations of independent claim 28, dependent claim 29 and dependent claim 30).

Claims 1-7 and 33-39 are allowable over the prior art of record.

The applicant's arguments with respect to the rejection of independent claim 27 under 35 U.S.C. §102(e) as being anticipated by Chen are incorrect.

First, contrary to the applicant's argument, although Chen discloses an embodiment wherein the p-channel transistor has lightly doped source and drain regions (see Chen's Figs. 1-10 embodiment, particularly Figs. 9-10), Chen also discloses an embodiment wherein the p-channel transistor does not have lightly doped source and drain regions (see Chen's Figs. 11-13 embodiment).

Furthermore, the applicant's argument: "The self-aligned lightly doped source and drain regions depicted in Figure 9 and described at column 5, lines 46-49 are presumably formed after the processing steps described in connection with Figures 12 and 13," is incorrect. Specifically, Chen's Figs. 1-10 embodiment's p-channel transistor comprises the shallow, lightly doped regions illustrated (but not numbered) in Figs. 9 and 10 because the p-channel transistor's source/drain implant is done though the thin sidewall gate oxide only (see Figs. 8 and 9). Chen's Figs. 11-13 embodiment's p-channel transistor, on the other hand, does not have shallow, lightly doped regions, as correctly depicted in Figs. 11-13, because the p-channel transistor's source/drain implant is done through the thin sidewall oxide together with additional, overlying spacer segments (see Fig. 11), which together prevent the formation of

lightly doped regions thereunder (much like insulated gate 28 concurrently prevents the formation of a p-region thereunder).

Finally, the applicant's argument that Chen does not disclose cited features of claim 27 falls with its primary argument ("The self-aligned lightly doped source and drain regions depicted in [Chen's] Figure 9 and described at column 5, lines 46-49 are presumably formed after the processing steps described in connection with Figures 12 and 13"), which was demonstrated to be incorrect in the preceding paragraph.

The applicant's arguments with respect to the rejection of independent claim 28 under 35 U.S.C. §102(e) as being anticipated by Chen are incorrect.

First, the applicant's arguments which repeat or parallel those made with respect to similar independent claim 27 are similarly incorrect, as explained above.

Furthermore, Chen does disclose independent claim 28's additional limitation "wherein the width of the gate electrode is less than a minimum channel length required for the p-channel transistor," as explained in the restatement of the rejection of claim 28. Note that the applicant's argument flows at least partly from its incorrect primary argument concerning Chen and thus falls therewith.

The applicant's argument with respect to the rejection of dependent claim 29 under 35 U.S.C. §102(e) as being anticipated by Chen is incorrect. Specifically, Chen does disclose dependent claim 29's additional limitation "wherein the first sidewall spacer regions have a width which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor," as explained in the restatement of the rejection of claim 29. Note that the applicant's argument flows at least partly from its incorrect primary argument concerning Chen and thus falls therewith.

Any inquiry concerning this communication should be directed to examiner Prenty at telephone number (703) 308-4939.

Mark Prenty
Mark V. Prenty
Primary Examiner

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